74LVC2G67-Q100

Bilateral switch

Rev. 1 — 23 September 2025 Product data sheet

1. General description

The 74LVC2G67-Q100 is a dual single pole, single-throw analog switch. Each switch has two input/output terminals (nY and nZ) and a digital enable input ($\overline{nE}$). When $\overline{nE}$ is HIGH, the analog switch is turned off. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 1.65 V to 5.5 V
- Very low ON resistance:
  - 7.5 Ω (typical) at V_{CC} = 2.7 V
  - 6.5 Ω (typical) at V_{CC} = 3.3 V
  - 6 Ω (typical) at V_{CC} = 5 V
- Switch current capability of 32 mA
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- CMOS low power consumption
- TTL interface compatibility at 3.3 V
- Latch-up performance meets requirements of JESD78 Class I
- Complies with JEDEC standards:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C (2.7 V to 3.6 V)
  - JESD36 (4.5 V to 5.5 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

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3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC2G67DP-Q100	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVC2G67DC-Q100	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74LVC2G67GT-Q100	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1

4. Marking

Table 2. Marking codes

Type number	Marking code[1]
74LVC2G67DP-Q100	V67
74LVC2G67DC-Q100	V67
74LVC2G67GT-Q100	V67

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

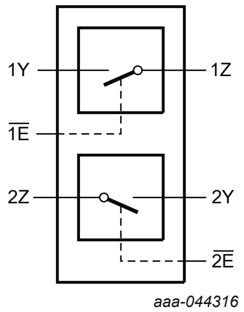


Fig. 1. Logic symbol

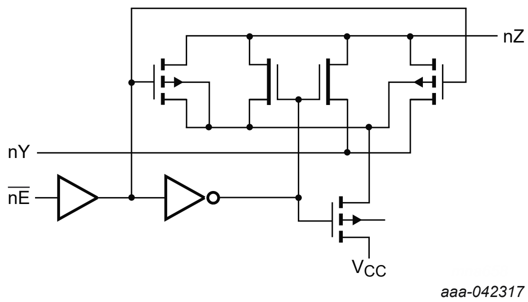
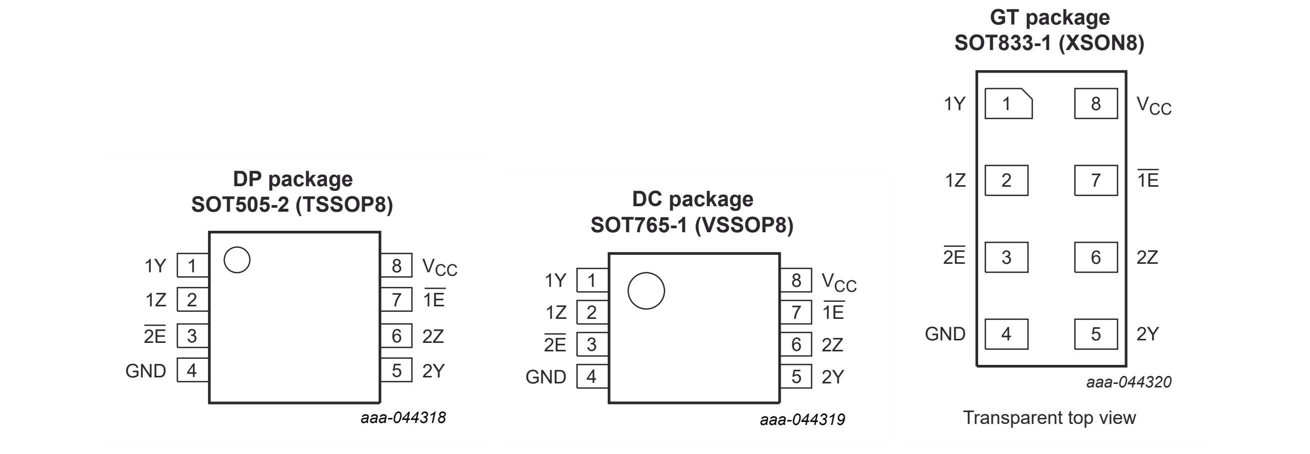


Fig. 2. Logic diagram (one switch)

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1Y	1	independent input or output
1Z	2	independent input or output
$\overline{2E}$	3	enable input (active LOW)
GND	4	ground (0 V)
2Y	5	independent input or output
2Z	6	independent input or output
$\overline{1E}$	7	enable input (active LOW)
V_{CC}	8	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input $\overline{nE}$	Switch
L	ON-state
H	OFF-state

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
V_I	input voltage	[1]	-0.5	+6.5	V
I_{IK}	input clamping current	V_I < -0.5 V or V_I > V_{CC} + 0.5 V	-50	-	mA
I_{SK}	switch clamping current	V_I < -0.5 V or V_I > V_{CC} + 0.5 V	-	±50	mA
V_{SW}	switch voltage	enable and disable mode [2]	-0.5	V_{CC} + 0.5	V
I_{SW}	switch current	V_{SW} > -0.5 V or V_{SW} < V_{CC} + 0.5 V	-	±50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C [3]	-	250	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.
[2] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed.
[3] For SOT505-2 (TSSOP8) package: P_{tot} derates linearly with 4.6 mW/K above 96 °C.
For SOT765-1 (VSSOP8) package: P_{tot} derates linearly with 4.9 mW/K above 99 °C.
For SOT833-1 (XSON8) package: P_{tot} derates linearly with 3.1 mW/K above 68 °C.

9. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_{SW}	switch voltage	[1]	0	V_{CC}	V
T_{amb}	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V [2]	-	20	ns/V
		V_{CC} = 2.7 V to 5.5 V	-	10	ns/V

[1] To avoid sinking GND current from terminal nZ when switch current flows in terminal nY, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal nZ, no GND current will flow from terminal nY. In this case, there is no limit for the voltage drop across the switch.
[2] Applies to control signal levels.

10. Static characteristics

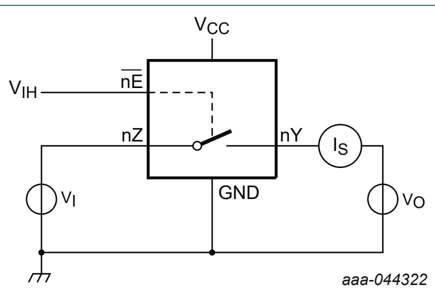
Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		-40 °C to +85 °C			-40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.65 × V_{CC}	-	-	0.65 × V_{CC}	-	V
		V_{CC} = 2.3 V to 2.7 V		1.7	-	-	1.7	-	V
		V_{CC} = 2.7 V to 3.6 V		2.0	-	-	2.0	-	V
		V_{CC} = 4.5 V to 5.5 V		0.7 × V_{CC}	-	-	0.7 × V_{CC}	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 V to 1.95 V		-	-	0.35 × V_{CC}	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		-	-	0.7	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V		-	-	0.8	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V		-	-	0.3 × V_{CC}	-	0.3 × V_{CC}	V
I_I	input leakage current	pin $n\overline{E}$; V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	[2]	-	±0.1	±1	-	±1	μA
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 5.5 V; see Fig. 3.	[2]	-	±0.1	±0.2	-	±0.5	μA
$I_{S(ON)}$	ON-state leakage current	V_{CC} = 5.5 V; see Fig. 4.	[2]	-	±0.1	±1	-	±2	μA
I_{CC}	supply current	V_I = 5.5 V or GND; V_{SW} = GND or V_{CC}; V_{CC} = 1.65 V to 5.5 V	[2]	-	0.1	4	-	4	μA
ΔI_{CC}	additional supply current	pin $n\overline{E}$; V_I = V_{CC} - 0.6 V; V_{SW} = GND or V_{CC}; V_{CC} = 5.5 V	[2]	-	5	500	-	500	μA
C_I	input capacitance			-	2.0	-	-	-	pF
$C_{S(OFF)}$	OFF-state capacitance			-	5.0	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance			-	9.5	-	-	-	pF

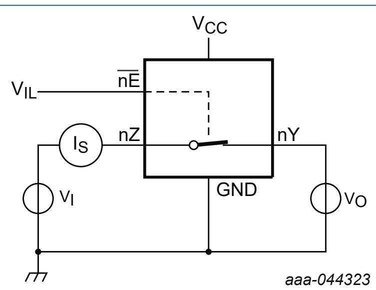
[1] All typical values are measured at T_{amb} = 25 °C.
[2] These typical values are measured at V_{CC} = 3.3 V.

10.1. Test circuits



V_I = V_{CC} or GND and V_O = GND or V_{CC}.

Fig. 3. Test circuit for measuring OFF-state leakage current



V_I = V_{CC} or GND and V_O = open circuit.

Fig. 4. Test circuit for measuring ON-state leakage current

10.2. ON resistance

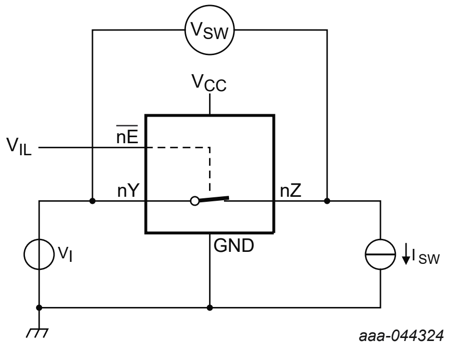
Table 8. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground 0 V); for graphs see Fig. 6 to Fig. 11.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$R_{ON(peak)}$	ON resistance (peak)	V_I = GND to V_{CC}; see Fig. 5.						
		I_{SW} = 4 mA; V_{CC} = 1.65 V to 1.95 V	-	34.0	130	-	195	Ω
		I_{SW} = 8 mA; V_{CC} = 2.3 V to 2.7 V	-	12.0	30	-	45	Ω
		I_{SW} = 12 mA; V_{CC} = 2.7 V	-	10.4	25	-	38	Ω
		I_{SW} = 24 mA; V_{CC} = 3 V to 3.6 V	-	7.8	20	-	30	Ω
		I_{SW} = 32 mA; V_{CC} = 4.5 V to 5.5 V	-	6.2	15	-	23	Ω
$R_{ON(rail)}$	ON resistance (rail)	V_I = GND; see Fig. 5						
		I_{SW} = 4 mA; V_{CC} = 1.65 V to 1.95 V	-	8.2	18	-	27	Ω
		I_{SW} = 8 mA; V_{CC} = 2.3 V to 2.7 V	-	7.1	16	-	24	Ω
		I_{SW} = 12 mA; V_{CC} = 2.7 V	-	6.9	14	-	21	Ω
		I_{SW} = 24 mA; V_{CC} = 3 V to 3.6 V	-	6.5	12	-	18	Ω
		I_{SW} = 32 mA; V_{CC} = 4.5 V to 5.5 V	-	5.8	10	-	15	Ω
		V_I = V_{CC}; see Fig. 5						
		I_{SW} = 4 mA; V_{CC} = 1.65 V to 1.95 V	-	10.4	30	-	45	Ω
		I_{SW} = 8 mA; V_{CC} = 2.3 V to 2.7 V	-	7.6	20	-	30	Ω
		I_{SW} = 12 mA; V_{CC} = 2.7 V	-	7.0	18	-	27	Ω
		I_{SW} = 24 mA; V_{CC} = 3 V to 3.6 V	-	6.1	15	-	23	Ω
		I_{SW} = 32 mA; V_{CC} = 4.5 V to 5.5 V	-	4.9	10	-	15	Ω
$R_{ON(flat)}$	ON resistance (flatness)	V_I = GND to V_{CC} [2]						
		I_{SW} = 4 mA; V_{CC} = 1.65 V to 1.95 V	-	26.0	-	-	-	Ω
		I_{SW} = 8 mA; V_{CC} = 2.3 V to 2.7 V	-	5.0	-	-	-	Ω
		I_{SW} = 12 mA; V_{CC} = 2.7 V	-	3.5	-	-	-	Ω
		I_{SW} = 24 mA; V_{CC} = 3 V to 3.6 V	-	2.0	-	-	-	Ω
		I_{SW} = 32 mA; V_{CC} = 4.5 V to 5.5 V	-	1.5	-	-	-	Ω

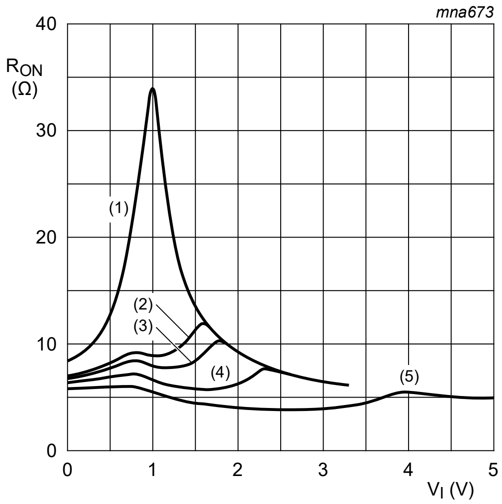
[1] Typical values are measured at T_{amb} = 25 °C and nominal V_{CC}.
[2] Flatness is defined as the difference between the maximum and minimum value of ON resistance measured at identical V_{CC} and temperature.

10.3. ON resistance test circuit and graphs



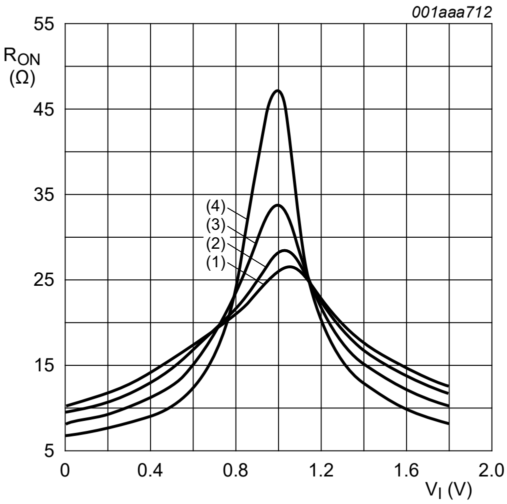
$R_{ON} = V_{SW} / I_{SW}$

Fig. 5. Test circuit for measuring ON resistance



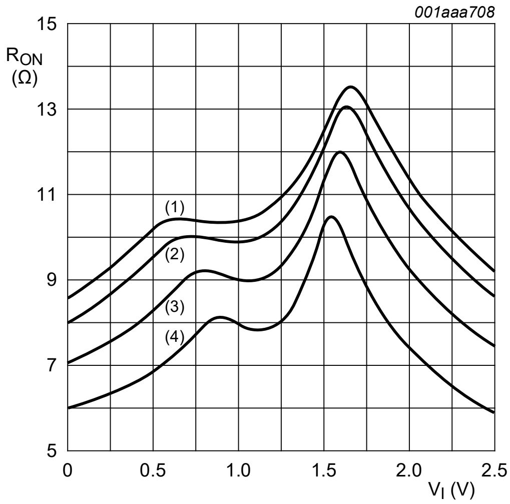
(1) V_{CC} = 1.8 V
(2) V_{CC} = 2.5 V
(3) V_{CC} = 2.7 V
(4) V_{CC} = 3.3 V
(5) V_{CC} = 5.0 V

Fig. 6. Typical ON resistance as a function of input voltage; T_{amb} = 25 °C



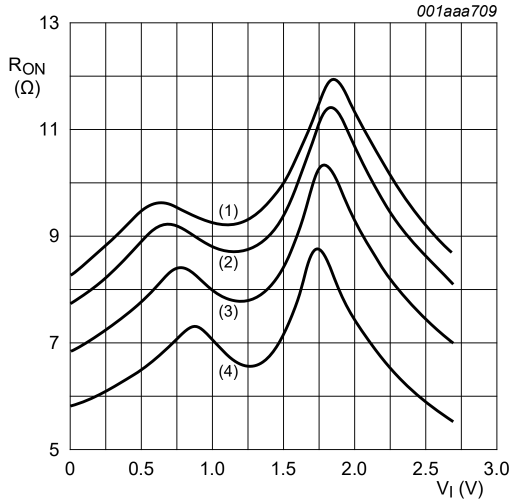
(1) T_{amb} = 125 °C
(2) T_{amb} = 85 °C
(3) T_{amb} = 25 °C
(4) T_{amb} = -40 °C

Fig. 7. ON resistance as a function of input voltage; V_{CC} = 1.8 V



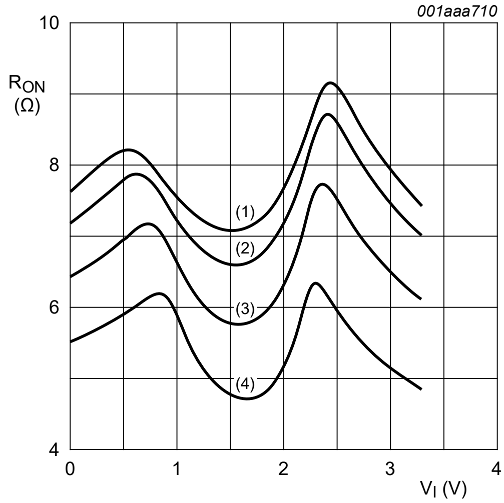
(1) T_{amb} = 125 °C
(2) T_{amb} = 85 °C
(3) T_{amb} = 25 °C
(4) T_{amb} = -40 °C

Fig. 8. ON resistance as a function of input voltage; V_{CC} = 2.5 V



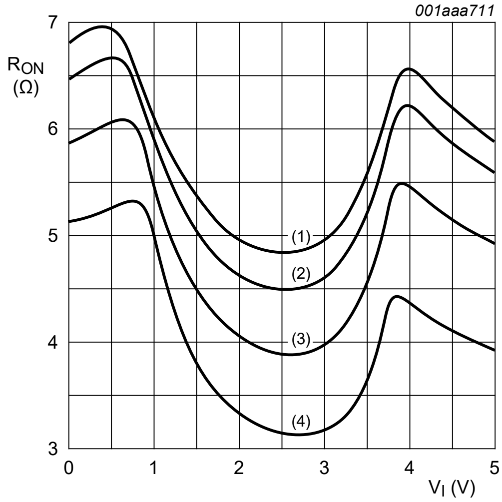
(1) T_{amb} = 125 °C
(2) T_{amb} = 85 °C
(3) T_{amb} = 25 °C
(4) T_{amb} = -40 °C

Fig. 9. ON resistance as a function of input voltage; V_{CC} = 2.7 V



(1) T_{amb} = 125 °C
(2) T_{amb} = 85 °C
(3) T_{amb} = 25 °C
(4) T_{amb} = -40 °C

Fig. 10. ON resistance as a function of input voltage; V_{CC} = 3.3 V



(1) T_{amb} = 125 °C
(2) T_{amb} = 85 °C
(3) T_{amb} = 25 °C
(4) T_{amb} = -40 °C

Fig. 11. ON resistance as a function of input voltage; V_{CC} = 5.0 V

11. Dynamic characteristics

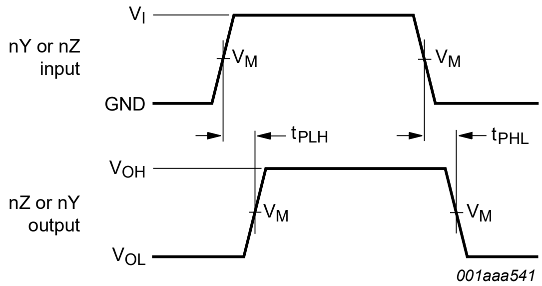
Table 9. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 14.

Symbol	Parameter	Conditions		-40 °C to +85 °C			-40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	nY to nZ or nZ to nY; see Fig. 12.	[2] [3]						
		V_{CC} = 1.65 V to 1.95 V		-	0.8	2.0	-	3.0	ns
		V_{CC} = 2.3 V to 2.7 V		-	0.4	1.2	-	2.0	ns
		V_{CC} = 2.7 V		-	0.4	1.0	-	1.5	ns
		V_{CC} = 3.0 V to 3.6 V		-	0.3	0.8	-	1.5	ns
		V_{CC} = 4.5 V to 5.5 V		-	0.2	0.6	-	1.0	ns
t_{en}	enable time	$n\overline{E}$ to nY or nZ; see Fig. 13.	[4]						
		V_{CC} = 1.65 V to 1.95 V		1.0	4.6	10	1.0	13.0	ns
		V_{CC} = 2.3 V to 2.7 V		1.0	2.7	5.6	1.0	7.5	ns
		V_{CC} = 2.7 V		1.0	2.7	5.0	1.0	6.5	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	2.4	4.4	1.0	6.0	ns
		V_{CC} = 4.5 V to 5.5 V		1.0	1.8	3.9	1.0	5.0	ns
t_{dis}	disable time	$n\overline{E}$ to nY or nZ; see Fig. 13.	[5]						
		V_{CC} = 1.65 V to 1.95 V		1.0	3.8	9.0	1.0	11.5	ns
		V_{CC} = 2.3 V to 2.7 V		1.0	2.1	5.5	1.0	7.0	ns
		V_{CC} = 2.7 V		1.0	3.5	6.5	1.0	8.5	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	3.0	6.0	1.0	8.0	ns
		V_{CC} = 4.5 V to 5.5 V		1.0	2.2	5.0	1.0	6.5	ns
C_{PD}	power dissipation capacitance	C_L = 50 pF; f_i = 10 MHz; V_I = GND to V_{CC}	[6]						
		V_{CC} = 2.5 V		-	9.0	-	-	-	pF
		V_{CC} = 3.3 V		-	11.0	-	-	-	pF
		V_{CC} = 5.0 V		-	15.7	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and nominal V_{CC}.
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
[3] Propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified capacitance when driven by an ideal voltage source (zero output impedance).
[4] t_{en} is the same as t_{PZH} and t_{PZL}.
[5] t_{dis} is the same as t_{PLZ} and t_{PHZ}.
[6] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \Sigma\{(C_L + C_{S(ON)}) \times V_{CC}{}^2 \times f_o\}$ where:
f_i = input frequency in MHz; f_o = output frequency in MHz;
C_L = output load capacitance in pF;
$C_{S(ON)}$ = maximum ON-state switch capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma\{(C_L + C_{S(ON)}) \times V_{CC}{}^2 \times f_o\}$ = sum of the outputs.

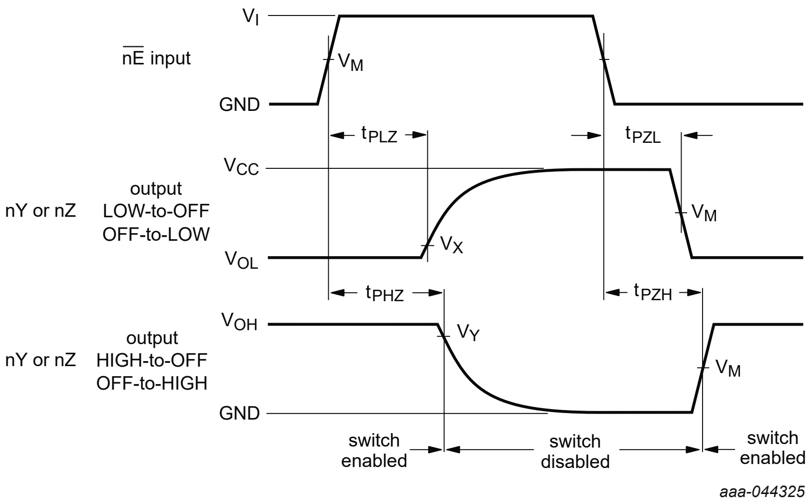
11.1. Waveforms and test circuit



Measurement points are given in Table 10.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 12. Input (nY or nZ) to output (nZ or nY) propagation delays



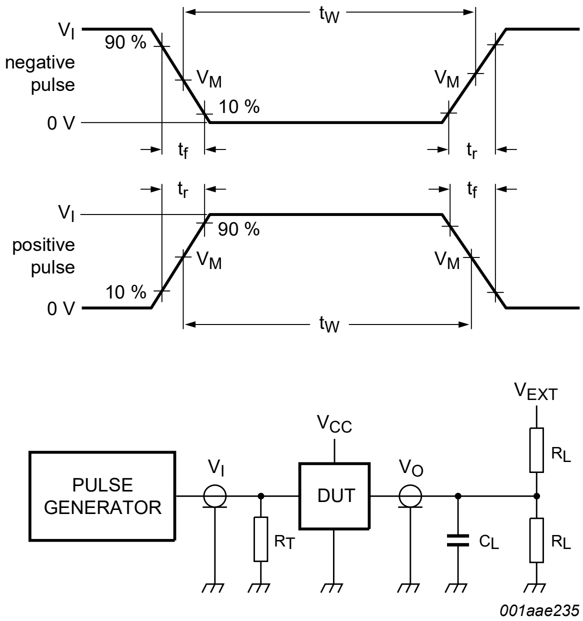
Measurement points are given in Table 10.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 13. Enable and disable times

Table 10. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
1.65 V to 1.95 V	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.3 V to 2.7 V	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V
3.0 V to 3.6 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V
4.5 V to 5.5 V	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 11.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

V_{EXT} = External voltage for measuring switching times.

Fig. 14. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 kΩ	open	GND	2 × V_{CC}
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	GND	2 × V_{CC}
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open	GND	2 × V_{CC}

11.2. Additional dynamic characteristics

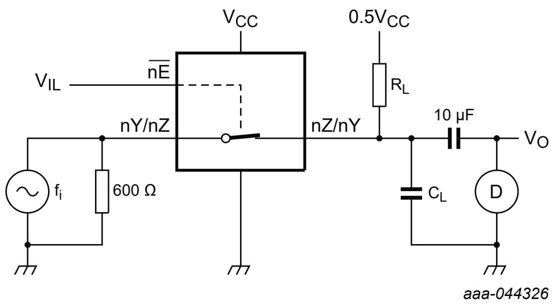
Table 12. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD	total harmonic distortion	R_L = 10 kΩ; C_L = 50 pF; f_i = 1 kHz; see Fig. 15.				
		V_{CC} = 1.65 V	-	0.032	-	%
		V_{CC} = 2.3 V	-	0.008	-	%
		V_{CC} = 3.0 V	-	0.006	-	%
		V_{CC} = 4.5 V	-	0.005	-	%
		R_L = 10 kΩ; C_L = 50 pF; f_i = 10 kHz; see Fig. 15.				
		V_{CC} = 1.65 V	-	0.068	-	%
		V_{CC} = 2.3 V	-	0.009	-	%
		V_{CC} = 3.0 V	-	0.008	-	%
		V_{CC} = 4.5 V	-	0.006	-	%
$f_{(-3dB)}$	-3 dB frequency response	R_L = 600 Ω; C_L = 50 pF; see Fig. 16.				
		V_{CC} = 1.65 V	-	135	-	MHz
		V_{CC} = 2.3 V	-	145	-	MHz
		V_{CC} = 3.0 V	-	150	-	MHz
		V_{CC} = 4.5 V	-	155	-	MHz
		R_L = 50 Ω; C_L = 10 pF; see Fig. 16.				
		V_{CC} = 1.65 V	-	200	-	MHz
		V_{CC} = 2.3 V	-	350	-	MHz
		V_{CC} = 3.0 V	-	410	-	MHz
		V_{CC} = 4.5 V	-	440	-	MHz
		R_L = 50 Ω; C_L = 5 pF; see Fig. 16.				
		V_{CC} = 1.65 V	-	> 500	-	MHz
		V_{CC} = 2.3 V	-	> 500	-	MHz
		V_{CC} = 3.0 V	-	> 500	-	MHz
		V_{CC} = 4.5 V	-	> 500	-	MHz
α_{iso}	isolation (OFF-state)	R_L = 600 Ω; C_L = 50 pF; f_i = 1 MHz; see Fig. 17.				
		V_{CC} = 1.65 V	-	-46	-	dB
		V_{CC} = 2.3 V	-	-46	-	dB
		V_{CC} = 3.0 V	-	-46	-	dB
		V_{CC} = 4.5 V	-	-46	-	dB
		R_L = 50 Ω; C_L = 5 pF; f_i = 1 MHz; see Fig. 17.				
		V_{CC} = 1.65 V	-	-37	-	dB
		V_{CC} = 2.3 V	-	-37	-	dB
		V_{CC} = 3.0 V	-	-37	-	dB
		V_{CC} = 4.5 V	-	-37	-	dB

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{ct}	crosstalk voltage	between digital inputs and switch; R_L = 600 Ω; C_L = 50 pF; f_i = 1 MHz; $t_r = t_f$ = 2 ns; see Fig. 18.				
		V_{CC} = 1.65 V	-	-	-	mV
		V_{CC} = 2.3 V	-	91	-	mV
		V_{CC} = 3.0 V	-	119	-	mV
		V_{CC} = 4.5 V	-	205	-	mV
Xtalk	crosstalk	between switches; R_L = 600 Ω; C_L = 50 pF; f_i = 1 MHz; see Fig. 19.				
		V_{CC} = 1.65 V	-	-	-	dB
		V_{CC} = 2.3 V	-	-56	-	dB
		V_{CC} = 3.0 V	-	-56	-	dB
		V_{CC} = 4.5 V	-	-56	-	dB
		between switches; R_L = 50 Ω; C_L = 5 pF; f_i = 1 MHz; see Fig. 19.				
		V_{CC} = 1.65 V	-	-	-	dB
		V_{CC} = 2.3 V	-	-29	-	dB
		V_{CC} = 3.0 V	-	-28	-	dB
		V_{CC} = 4.5 V	-	-28	-	dB
Q_{inj}	charge injection	C_L = 0.1 nF; V_{gen} = 0 V; R_{gen} = 0 Ω; f_i = 1 MHz; R_L = 1 MΩ; see Fig. 20.				
		V_{CC} = 1.8 V	-	3.3	-	pC
		V_{CC} = 2.5 V	-	4.1	-	pC
		V_{CC} = 3.3 V	-	5.0	-	pC
		V_{CC} = 4.5 V	-	6.4	-	pC
		V_{CC} = 5.5 V	-	7.5	-	pC

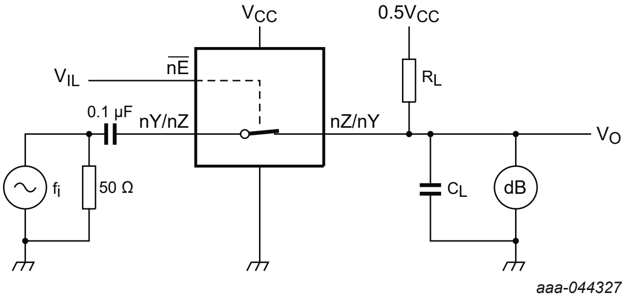
11.3. Test circuits



Test conditions:

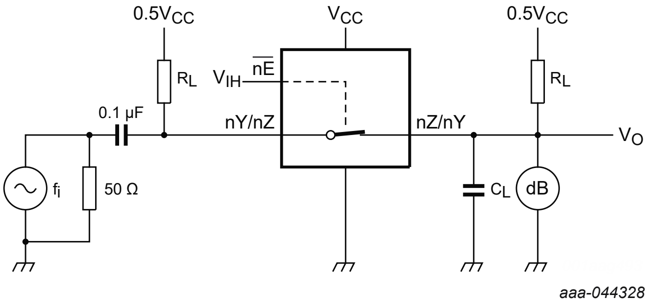
V_{CC} = 1.65 V: V_i = 1.4 V (p-p)
V_{CC} = 2.3 V: V_i = 2 V (p-p)
V_{CC} = 3 V: V_i = 2.5 V (p-p)
V_{CC} = 4.5 V: V_i = 4 V (p-p)

Fig. 15. Test circuit for measuring total harmonic distortion



Adjust f_i voltage to obtain 0 dBm level at output. Increase f_i frequency until dB meter reads -3 dB.

Fig. 16. Test circuit for measuring the frequency response when switch is in ON-state



Adjust f_i voltage to obtain 0 dBm level at input.

Fig. 17. Test circuit for measuring isolation (OFF-state)

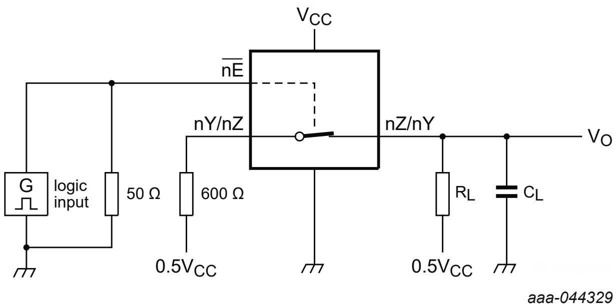
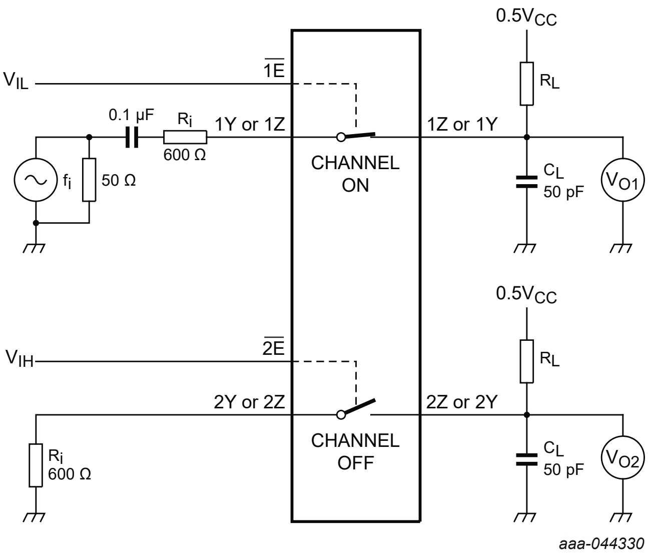
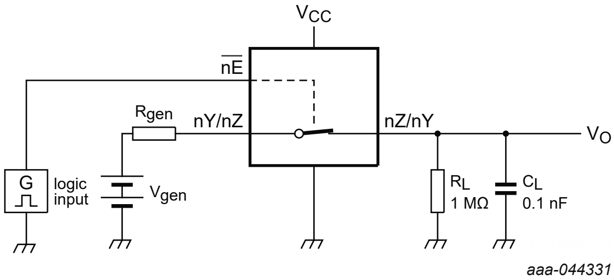


Fig. 18. Test circuit for measuring crosstalk voltage (between digital inputs and switch)

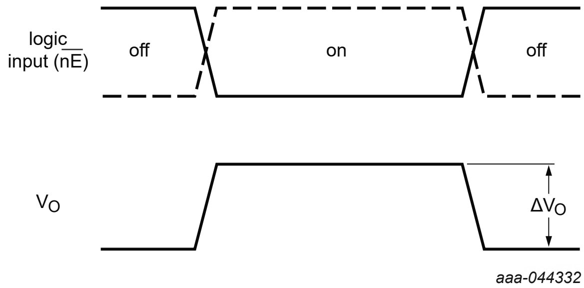


$20 \log_{10} (V_{O2} / V_{O1})$ or $20 \log_{10} (V_{O1} / V_{O2})$.

Fig. 19. Test circuit for measuring crosstalk between switches



a. Test circuit



b. Input and output pulse definitions

$Q_{inj} = \Delta V_O \times C_L$

ΔV_O = output voltage variation

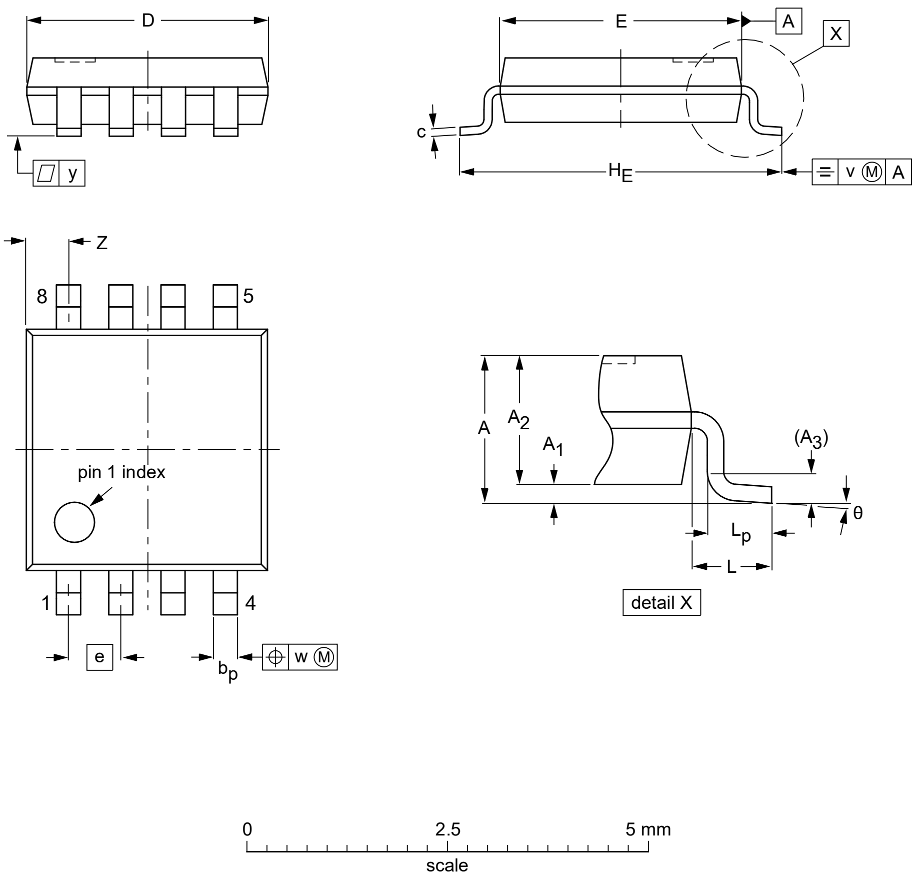
R_{gen} = generator resistance

V_{gen} = generator voltage

Fig. 20. Test circuit for measuring charge injection

12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	v	w	y	Z(1)	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

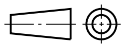
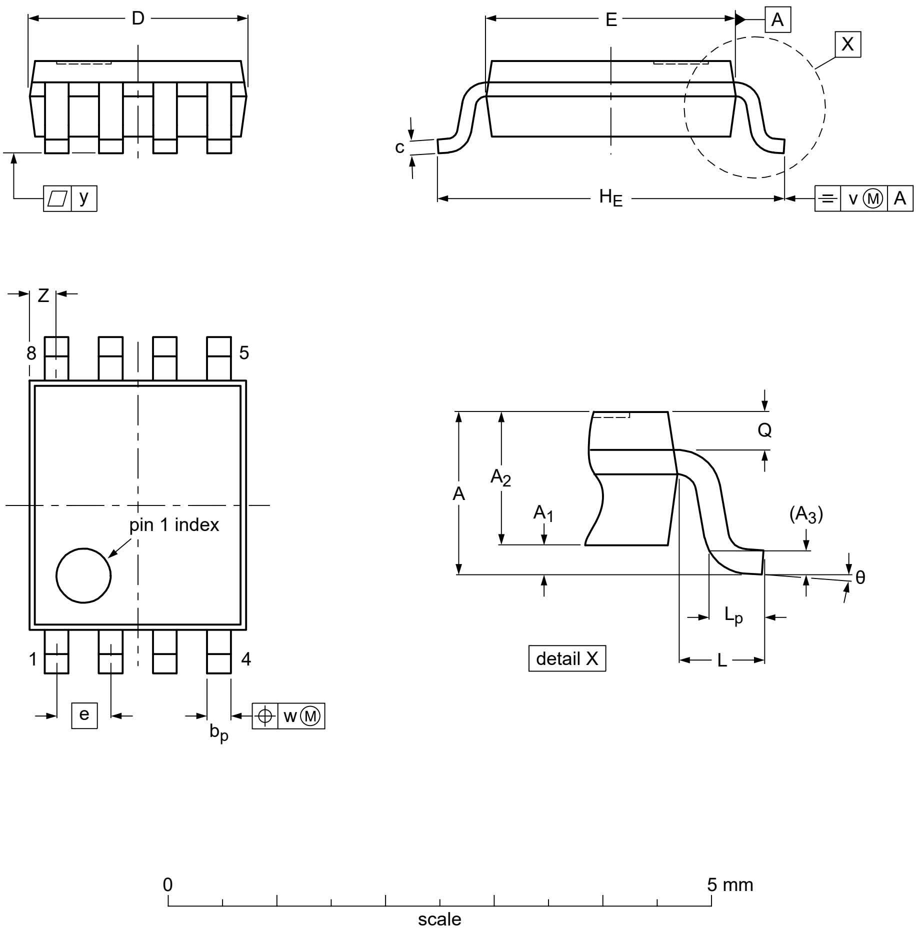
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		- - -				02-01-16

Fig. 21. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm **SOT765-1**



Dimensions (mm are the original dimensions)

Unit		A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	max		0.15	0.85		0.27	0.23	2.1	2.4		3.2		0.40	0.21				0.4	8°
	nom	1			0.12					0.5		0.4			0.2	0.08	0.1		
	min		0.00	0.60		0.17	0.08	1.9	2.2		3.0		0.15	0.19				0.1	0°

Note

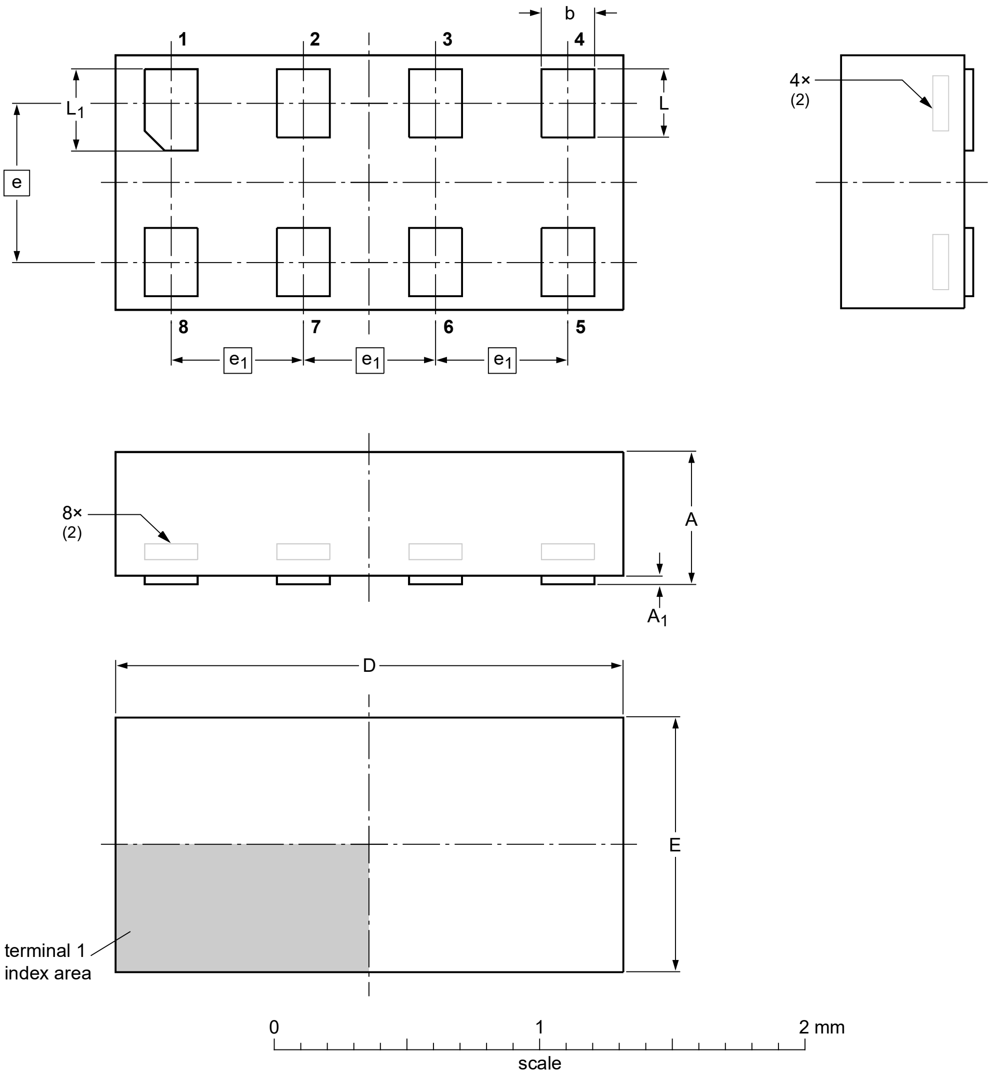
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

sot765-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				~~07-06-02~~ 16-05-31

Fig. 22. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm **SOT833-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max	A_1 max	b	D	E	e	e_1	L	L_1
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

Notes

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

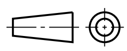
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT833-1	- - -	MO-252	- - -			~~07-11-14~~ 07-12-07

Fig. 23. Package outline SOT833-1 (XSON8)

13. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC2G67_Q100 v.1	20250923	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Contents